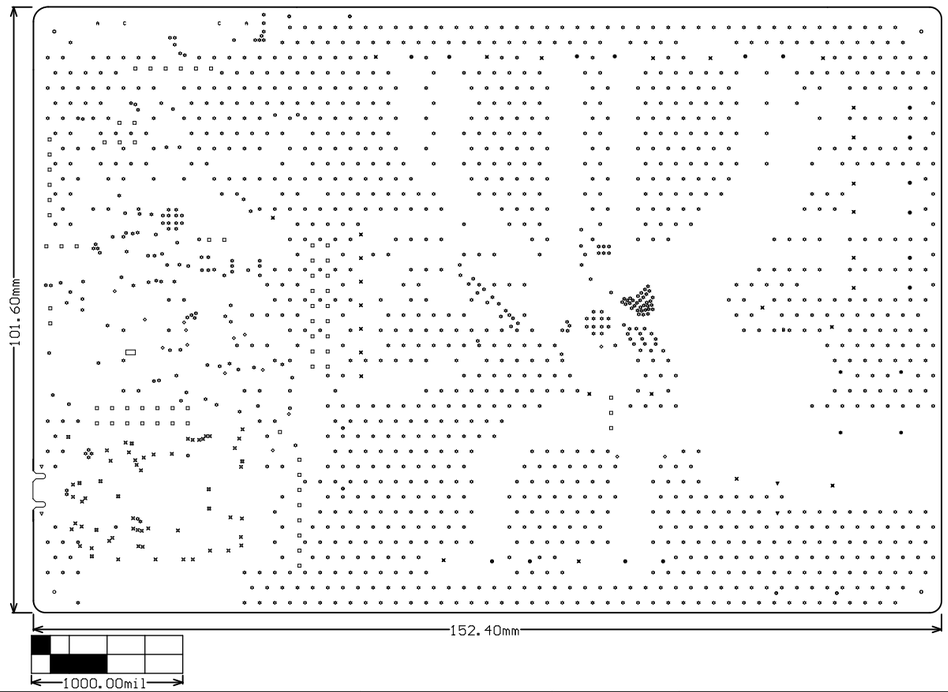
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4 High Tg	59.20mil	4.8	
2	Mid-Layer 1		1.40mil		
	Dielectric2	FR-4	12.60mil	4.8	
3	Mid-Layer 2		1.40mil		
	Dielectric3	FR-4	12.60mil	4.8	
4	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
C	2	59,00mil (1.499mm)	NPTH	Round	Top Layer - Bottom Layer	
	1416	7,87mil (0,200mm)	PTH	Round	Top Layer - Bottom Layer	
	49	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
	10	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	
	15	16.00mil (0.406mm)	PTH	Round	Top Layer - Bottom Layer	
B	1	17.72mil (0.450mm)	PTH	Round	Top Layer - Bottom Layer	
	2	35,43mil (0,900mm)	PTH	Round	Top Layer - Bottom Layer	
	68	40,00mil (1,016mm)	PTH	Round	Top Layer - Bottom Layer	
	6	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
	16	59.06mil (1.500mm)	PTH	Round	Top Layer - Bottom Layer	
	4	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
	28	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
A	2	120,00mil (3,048mm)	PTH	Round	Top Layer - Bottom Layer	
	3	169,29mil (4,300mm)	PTH	Round	Top Layer - Bottom Layer	
	1	177,17mil (4,500mm)	PTH	Round	Top Layer - Bottom Layer	
	2	23,62mil (0,600mm)	PTH	Slot	Top Layer - Bottom Layer	
	1625 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-4 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: MD085_DRV8001
DESIGNED FOR: Public Release
FILE NAME: MD085_DRV800x.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MD085	REV: E1	SVN REV: Unknown revision
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 1/14/2025 1:46:22 PM	TEXAS INSTRUMENTS	

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ENGINEER: Shinya Morita	LAYOUT BY: Keerthi Kumanan
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.7.2.38